REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-76 are presently active in this case, Claims 32-34, 37, 56, 57, 60, 61, and 76 having been amended by way of the present Amendment.

Claims 19-31, 38-55, 62, 63, 65, 68, 71, and 74 have been allowed. Additionally, Claims 3-11 and 14-18 haven been indicated as containing allowable subject matter.

In the outstanding Official Action, Claim 8 was objected to for being identical to Claim 7. The Applicant respectfully traverses this objection. Claim 7 recites the phrase "writing operation," while Claim 8 recites the phrase "reading operation." Therefore, Claims 7 and 8 are not identical, and the Applicant respectfully requests the withdrawal of the objection to Claim 8.

Claims 32-37 and 56-61 were objected to under 37 CFR 1.75(c) for being in improper multiple dependent form. Claims 32-34, 37, 56, 57, 60, and 61 have been amended to remove all the improper multiple dependencies. Accordingly, the Applicant requests the withdrawal of the objections to Claims 32-37 and 56-61.

Claims 32-37 and 56-61 were indicated as being allowable if the objections under 37 CFR 1.75(c) were overcome. As noted above, the objections to these claims have been overcome, and therefore the Applicant submits that Claims 32-37 and 56-61 are in condition for allowance.

Claims 1, 2, 12, 13, 64, 66, 67, 69, 70, 72, 73, 75, and 76 were rejected under 35 U.S.C. 102(a) as being anticipated by Saruta et al. (EP 1 004 450 A2). For the reasons discussed below, the Applicant traverses the anticipatory rejection.

Firstly, the Applicant notes that the Official Action indicates that U.S. Patent No. 6,798,997 corresponds to the Saruta et al. reference being cited. However, U.S. Patent No. 6,798,997 relates to a Supply Ordering Apparatus by Hayward et al., which does not appear the correct citation. Instead, the Applicant notes that EP 1 004 450 A2, which is currently of record, appears to be the correct citation. Clarification of this discrepancy is respectfully requested in the next Official Action. For the purposes of this response, the arguments are directed to EP 1 004 450 A to Saruta et al.

In the Office Action, the Saruta et al. reference is indicated as anticipating each of independent Claims 1, 12, 64, 66, 67, 70, 72, 73, 75, and 76. However, the Applicant notes that a claim is anticipated only if each and every element as set forth in the claims is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). As will be demonstrated below, the Saruta et al. reference clearly does not meet each and every limitation of the independent Claims 1, 12, 64, 66, 67, 70, 72, 73, 75, and 76.

Claims 1 and 12 recite a container and device, respectively, that are attached to a reset signal line and comprise a storage element having a plurality of non-volatile storage areas that are sequentially accessed, and a storage element control unit that is initialized at a first level of the input reset signal and carries out a writing/reading operation of data into and from the storage element according to the data signal synchronously with the input clock signal

when the reset signal is switched over to a second level. Claims 64 and 70 recite methods of gaining access to a storage device that connects with a reset signal line via a bus, where the method comprises outputting a reset signal to the reset signal line, and transmitting a data array including identification information, which is assigned to the storage device, and a write/read command to the data signal line synchronously with a clock signal. Claims 66, 67, 72, and 73 recite methods comprising steps of resetting a count on an address counter to an initial value and prohibiting increment of the count synchronously with a clock signal, in response to detection of a reset signal, setting a direction of data transfer with regard to a data bus, allowing increment of the count on the address counter synchronously with the clock signal after completion of the settings of the directions of data transfer, and reading or writing according to the count on the address counter. Claim 75 recites a non-volatile storage device that connects with a clock signal line, a data signal line, and a reset signal line and is initialized in response to a reset signal input via the reset signal line. Claim 76 recites a printing material container comprising a storage element configured to be responsive to a reset signal input therein and having a storage area of an identification information, and a writable data area, in which data are writable, after the storage area of the identification information.

The Applicant submits that the Saruta et al. reference does not disclose all of the above features recited in Claims 1, 12, 64, 66, 67, 70, 72, 73, 75, and 76. More specifically, the Saruta et al. reference does not disclose a reset signal, reset signal line, or reset signal terminal as recited, or a method or apparatus configured to utilize such a reset signal in the manner recited in these claims.

The Saruta et al. reference describes a storage element (80) of ink cartridges. The storage unit (80) includes a memory cell (81), a read/write controller (82), and an address counter (83). The read/write controller (82) is a circuit that controls reading and writing operations of data from and into the memory cell (81), and notably the read/write controller (82) is not connected to the chip select signal line and thus cannot receive the chip select signal.

The controller (46) of the print controller (40) is configured to make a chip select signal (CS), which sets the storage element (80) in an enabling state, in a high level at step ST21. While the chip select signal (CS) is kept at the low level, the count on the address counter (83) is set equal to zero. When the chip select signal (CS) is set to the high level, the address counter (83) is enabled to start the count. The controller (46) then generates a required number of pulses of the clock signal (CLK) to specify an address, at which data are written, at step ST22. The address decoder (95) incorporated in the print controller (40) is used to determine the required number of pulses of the clock signal (CLK). The address counter (83) included in the storage element (80) counts up in response to the required number of pulses of the clock signal (CLK) thus generated. During this process, a read/write signal (R/W) is kept in a low level. This means that an instruction of reading data is given to the memory cell (81). Dummy data are accordingly read synchronously with the output clock signal (CLK).

After the address counter (83) counts up to the specified address for writing data, the controller (46) carries out an actual writing operation at step ST23. The writing operation switches the read/write signal (R/W) to the high level, outputs one-bit data to a data terminal

I/O, and changes the clock signal (CLK) to a high active state on the completion of data output. While the read/write signal (R/W) is in the high level, data (DATA) of the data terminal I/O are written into the memory cell (81) of the storage element (80) synchronously with a rise of the clock signal (CLK). Although the writing operation starts synchronously with a fifth pulse of the clock signal (CLK) in the example of FIG. 7B, this only describes the general writing procedure. The writing operation of required data, for example, the remaining quantity of ink, may be carried out at any pulse, for example, at a first pulse, of the clock signal (CLK) according to the requirements.

Thus, the Saruta et al. reference does not disclose the simplified configuration and methods of the present invention in which a reset signal that can be used to control writing/reading operation of data itself. As indicated by the description of the Saruta reference set forth above, numerous signals must be sent between the print controller (40) and the storage element (80) in order to produce an actual writing operation via read/write controller (82). The Saruta et al. reference does not describe, however, utilizing a reset signal to initialize a storage element control unit, as recited in Claim 1 of the present application, for example. Not only does the Saruta et al. reference not disclose such a reset signal, but also the chip select signal (CS), which is cited for the reset signal, is not provided to the read/write controller (82), but rather numerous signals are used to ultimately operate the read/write controller (82).

Thus, the Applicant respectfully submits that the Saruta et al. reference does not disclose a reset signal line and a storage element having the features recited in Claims 1 and 12, outputting a reset signal to a reset signal line and transmitting a data array recited in

Claims 64 and 70, resetting a count on an address counter to an initial value and prohibiting increment of the count synchronously with a clock signal, in response to detection of a reset signal and subsequent steps recited in Claims 66, 67, 72, and 73, storage device that connects with a clock signal line, a data signal line, and a reset signal line and is initialized in response to a reset signal input via the reset signal line recited in Claim 75, and a storage element configured to be responsive to a reset signal input therein recited in Claim 76.

Accordingly, the Applicant respectfully requests the withdrawal of the anticipation rejection of Claims 1, 12, 64, 66, 67, 70, 72, 73, 75, and 76.

The rejected dependent claims are considered allowable for the reasons advanced for the independent claim from which they depend.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully Submitted,

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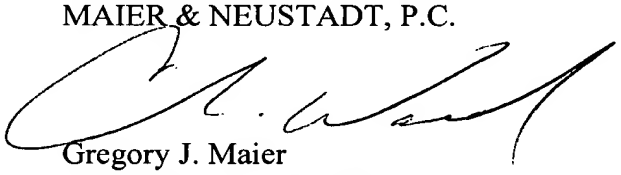

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